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Process Tolerant Single Photolithography/Implantation 120-Zone Junction Termination Extension

V. Veliadis[1,a], M. Snook[1], H. Hearne[1], B. Nechay[1], S. Woodruff[1], C. Lavoie[1], C. Kirby[1], E. Imhoff[2,b], J. White[3], S. Davis[3,c]

[1]Northrop Grumman Electronic Systems, Linthicum, MD 21090, USA

[2]US Naval Research Laboratory, 4555 Overlook Avenue SW, Washington, DC 20375

[3]US Army TARDEC, 6501 E. 11 Mile Road, Warren, MI 48397-5000

[a]victor.veliadis@ngc.com, [b]eugene.imhoff@nrl.navy.mil, [c]stuart.m.davis.civ@mail.mil

Keywords: Junction termination extension, JTE, multiple-zone JTE, edge termination, single implant, single photolithography, blocking voltage, high voltage, diode, silicon carbide, SiC, PiN.

Abstract. The multiple-zone junction termination extension (MJTE) is a widely used SiC edge termination technique that reduces sensitivity to implantation dose variations. It is typically implemented in multiple lithography and implantation events. To reduce process complexity, cycle time, and cost, a single photolithography/implantation (P/I) MJTE technique was developed and diodes with 3-zone and 120-zone JTEs were fabricated on the same wafer. Here, the process tolerance of the single (P/I) MJTE technique is evaluated by performing CCD monitored blocking voltage measurements on diodes from the same wafer with the 3-zone and 120-zone single (P/I) JTE. The 3-zone JTE diodes exhibited catastrophic localized avalanches at the interface between the 2nd and 3rd zones due to abrupt zone transitions. Diodes with the smooth transitioning 120-zone JTE exhibited no CCD detectable avalanches in their JTE regions up to the testing limit of 12 kV. Under thick dielectric (deposited for on-wafer diode interconnection), diodes with the single P/I 3-zone JTE failed due to significant loss of high-voltage capability, while their 120-zone JTE diode counterparts were minimally affected. Overall, the single (P/I) 120-zone JTE provides a process-tolerant and robust single P/I edge termination at no additional fabrication labor.

Introduction

The theoretical breakdown voltage of 4H-SiC can be reached in high-voltage power devices only when a properly designed edge termination structure is used to reduce electric field crowding at the edges of the device. In a conventional single-zone JTE [1], the optimum implantation dose range for maximizing breakdown voltage is typically too narrow. Thus, particularly at higher voltages, the use of multiple-zone JTEs reduces sensitivity to dose variations resulting in more process tolerance. An MJTE achieves high breakdown voltage by varying the dose of implanted ions from high to low in the lateral direction. MJTEs typically require several photolithography/implantation events, which increase process cycle time, complexity, and cost. As a result, single implantation multiple-zone edge terminations are being developed including gray-scale photolithographic masking [2], and etched mesa and dielectric techniques [3]. Recently, 6 kV PiN diodes with MJTEs fabricated in a single P/I event were reported [4]. It was shown that PiN diodes with single P/I 3-zone and 120-zone JTE designs achieved yields and breakdown voltages that compared favorably to those of control diodes terminated with the more labor intensive three P/I events MJTE. It was further shown that the fabrication labor of the single P/I MJTE technique is independent of the number of zones. In this work, we investigate the process tolerance of the single P/I JTE technique by performing CCD monitored blocking voltage measurements on 3-zone and 120-zone single P/I JTE diodes fabricated on the same wafer.

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14. ABSTRACT

The multiple-zone junction termination extension (MJTE) is a widely used SiC edge termination technique that reduces sensitivity to implantation dose variations. It is typically implemented in multiple lithography and implantation events. To reduce process complexity, cycle time, and cost, a single photolithography/implantation (P/I) MJTE technique was developed and diodes with 3-zone and 120-zone JTEs were fabricated on the same wafer. Here, the process tolerance of the single (P/I) MJTE technique is evaluated by performing CCD monitored blocking voltage measurements on diodes from the same wafer with the 3-zone and 120-zone single (P/I) JTE. The 3-zone JTE diodes exhibited catastrophic localized avalanches at the interface between the 2nd and 3rd zones due to abrupt zone transitions. Diodes with the smooth transitioning 120-zone JTE exhibited no CCD detectable avalanches in their JTE regions up to the testing limit of 12 kV. Under thick dielectric (deposited for on-wafer diode interconnection), diodes with the single P/I 3-zone JTE failed due to significant loss of high-voltage capability, while their 120-zone JTE diode counterparts were minimally affected. Overall, the single (P/I) 120-zone JTE provides a processtolerant and robust single P/I edge termination at no additional fabrication labor.

15. SUBJECT TERMS
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Results and Discussion

10-kV class PiN diodes with an active area of 0.087 cm^2 (0.17 cm^2 total area) were fabricated with single P/I 3-zone and 120-zone JTE designs on the same wafer. 4H-SiC n+ substrates with nominal 100 μm epitaxial n- drift layers doped to 5 x 10^{14} cm^{-3} were used. Even row diodes were terminated with the single P/I 3-zone JTE, while odd row diodes had the single P/I 120-zone edge termination. The single P/I MJTE was implemented by forming a pattern of finely graduated windows, etched into a dielectric mask, that decrease in area with each successive zone from the device mesa to the outermost periphery of the MJTE region [4]. The pattern was transferred to the dielectric via reactive ion etching. Each zone represents a percent of implant dose penetration from 100% (full implant dose) at zone 1 to 25% for the outermost zone. An optical micrograph of a PiN diode with a 120 zone JTE is shown in Figure 1. The scanning electron micrographs (SEM) at the top of Fig. 1, illustrate regions of approximately 40% and 80% implant dose penetration. The 40% region is comprised of windows etched in the dielectric film, Fig. 1(a), which filter a significant portion of the implantation dose. The pillars of dielectric in the 80% zone, Fig. 1(b), filter only a small percentage of implanted dopants. Using a combination of dielectric pillars and etched windows eases critical dimension requirements. Aluminum ion implantation at elevated temperature formed the MJTE regions with a subsequent high temperature anneal activating the dopants and re-crystallizing the material.

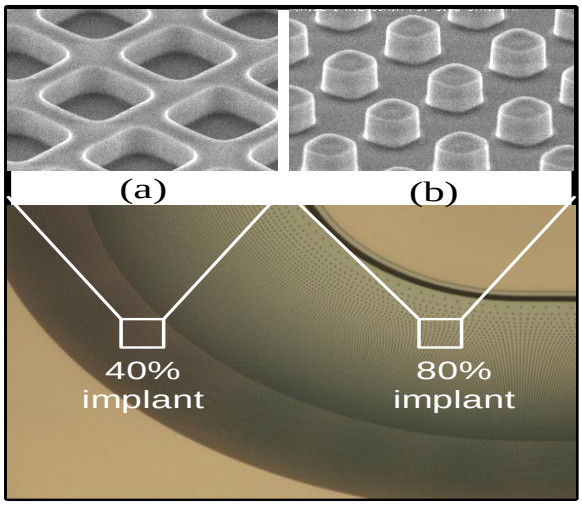

Fig. 1. Optical image of the 120 zone dielectric mask (bottom), and SEM images (top) showing patterns designed for 40% (a), and 80% (b) implant-dose penetrations, with respect to the implant dose at the anode edge of the PiN diode.

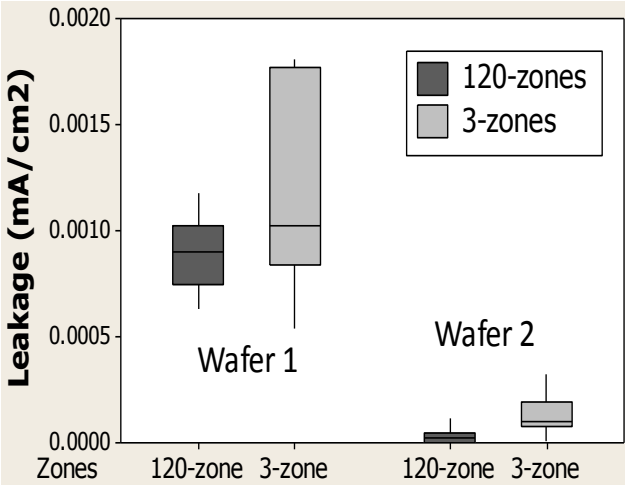

Fig. 2. Statistical leakage current-density at 8 kV for PiN diodes of two wafers, with single photolithography/implantation 3-zone and 120-zone JTEs fabricated on the same wafer. Diodes with the 3-zone JTE exhibited higher leakage current and variance.

PiN diodes with single P/I 3-zone and 120-zone JTE designs, fabricated on the same wafer, were pulsed to 10 kV. Statistical data of leakage current density (measured at 8 kV), for diodes that blocked 10 kV with leakage current densities below 0.2 mA/cm^2, is presented in Fig. 2 for two representative wafers. Diodes with the 3-zone JTE exhibited higher leakage current and variance, which is attributed to the more abrupt zone transitions in the 3-zone JTE. To further investigate the performance of the single P/I MJTE designs, images of diodes in blocking state were captured using a high sensitivity CCD camera. The PiN diodes selected for CCD testing had low leakage currents with sharp onsets of breakdown. Three 3-zone JTE diodes were tested and exhibited catastrophic localized avalanches at the interface between the 2^{nd} and 3^{rd} zone at blocking voltages of 3.5 kV, 6.5 kV, and 8 kV.

A CCD camera image of a PiN diode with a single photolithography/implantation 3-zone JTE in the 3.5 kV blocking state is shown in Fig. 3. A localized avalanche can be observed at the interface between the 2nd and 3rd JTE zones (see area surrounded by the rectangle), which indicates that the diode is prone to catastrophic voltage breakdown at this location. This is attributed to the sharp transition between the pillars of zone 2 and the etched windows of zone 3, Fig. 4.

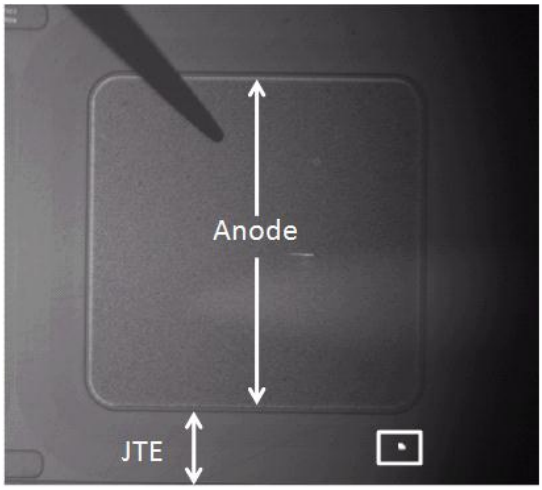

Fig. 3. CCD image of a PiN diode with a single P/I 3-zone JTE in the 3.5 kV blocking state. Localized avalanche can be observed at the interface between the 2nd and 3rd JTE zones (see inside the rectangle).

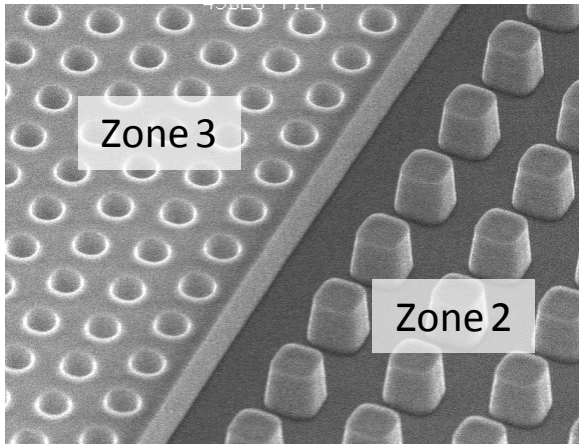

Fig. 4. SEM image showing the abrupt 2nd to 3rd JTE zone transition of the 3-zone single P/I JTE. Slight variations in lithographic patterning can result in significant shifts of effective dose penetration.

Five 120-zone JTE diodes were also tested and exhibited no CCD detectable avalanche in their JTE regions up to the testing limit of 12 kV. The smooth zone transitions of the 120-zone JTE resulted in a more process tolerant and as such more robust MJTE. Representative 120-zone JTE PiN diode reverse leakage data, collected under CCD monitored blocking voltage testing, are presented in the graph of Fig. 5. As the 3-zone and 120-zone single P/I JTEs were implemented on the same wafer, the results indicate that the 120-zone JTE provides a superior edge termination structure at no additional fabrication labor.

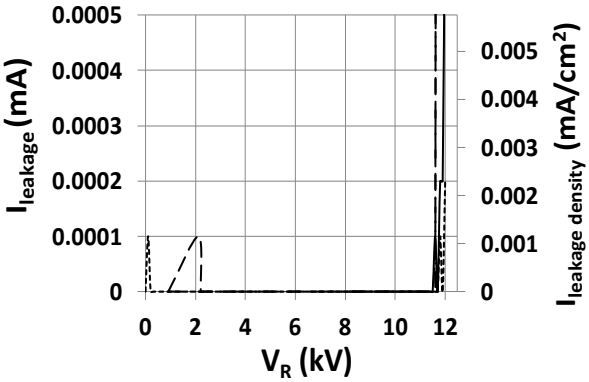

Fig. 5. Single P/I 120-zone JTE PiN diode reverse leakage data, collected under CCD monitored blocking voltage testing. The diodes exhibited no CCD detectable avalanche in their JTE regions up to the testing limit of 12 kV.

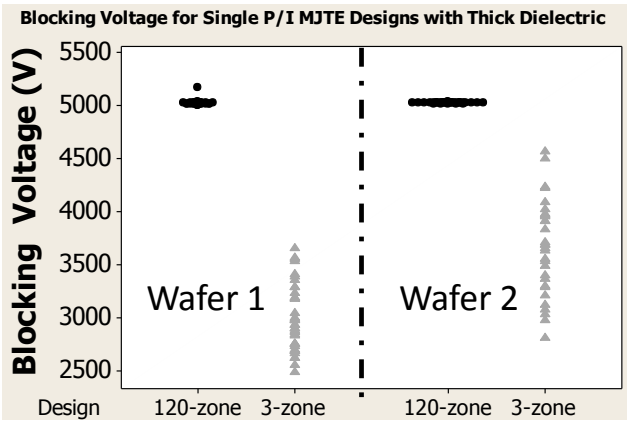

Fig. 6. Statistical blocking-voltage data for PiN diodes of two wafers with thick dielectric. Diodes with single P/I 3-zone JTEs failed at the leakage current density of 0.2 mA/cm^2 due to drastic breakdown voltage drops. Diodes with the 120-zone JTE exceeded their 5 kV specification at leakage current densities of less than 0.03 mA/cm^2.

In experiments of on-wafer PiN diode interconnection [1], wafers with single P/I 3-zone and 120-zone JTE diodes had a thick dielectric (designed to withstand high-voltage on-wafer interconnected diode operation) uniformly deposited on their surface. Subsequently, windows were opened in the dielectric to expose the anodes of known good diodes and blocking voltage measurements were performed with the single P/I MJTEs now buried under the thick dielectric. It is well known that dielectric charges accumulating at the JTE-dielectric interface can interfere with JTE operation and degrade its performance [5-6]. While all the diodes with single P/I 3-zone JTEs failed due to significant loss of high voltage capability, the 120-zone JTE diodes were minimally affected. Statistical blocking-voltage data for PiN diodes of two wafers, with thick dielectric for on-wafer interconnection, are shown in Fig. 6. All diodes with single P/I 3-zone JTEs failed at the leakage current density of 0.2 mA/cm^2 due to drastic breakdown voltage drops. Diodes with the 120-zone JTE exceeded their 5 kV specification at very low leakage current densities of less than 0.03 mA/cm^2, which confirms the robustness of the single P/I 120-zone edge termination.

Summary

The process tolerance of the single photolithography/implantation MJTE technique was evaluated by performing CCD monitored blocking voltage measurements on diodes with 3-zone and 120-zone JTEs fabricated on the same wafer. The single P/I 3-zone JTE diodes exhibited catastrophic localized avalanches at the interface between the 2^{nd} and 3^{rd} zones due to the abrupt zone transitions. Diodes with the smooth transitioning single P/I 120-zone JTE exhibited no CCD detectable avalanches in their JTE regions up to the testing limit of 12 kV. Overall, the 120-zone JTE provides a process tolerant single photolithography/implantation edge termination at no additional fabrication labor.

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